IN THE CLAIMS

Please amend the claims as follows:

1. (original) An electronic circuit comprising:

first and second combinational logic blocks; and

a latch positioned between the combinational logic blocks;

wherein the electronic circuit is adapted to operate in a normal mode in which the latch is opened and closed in response to an enable signal, and a test mode in which the latch is held open.

2. (original) An electronic circuit as claimed in claim 1, further comprising a latch control circuit connected to the latch, the latch control circuit being adapted to control the latch with the enable signal when the electronic circuit is in the normal mode, and to hold the latch open when the electronic circuit is in the test mode.

3. (original) An electronic circuit as claimed in claim 2, wherein the latch control circuit receives a signal indicating the mode of operation of the electronic circuit.

4. (currently amended) An electronic circuit as claimed in ~~one of claims 1 to 3~~claim 1, further comprising means for inserting test

data into the first combinational logic block when the electronic circuit is in the test mode; the test data being processed by the first and second combinational logic blocks as though they are a single combinational logic block.

5. (original) An electronic circuit as claimed in claim 4, further comprising means for reading the processed test data from the second combinational logic block when the electronic circuit is in the test mode.

6. (original) A method of operating an electronic circuit, the electronic circuit comprising first and second combinational logic blocks and a latch positioned between the blocks, the method comprising:

operating the electronic circuit in a normal mode in which the latch is opened and closed in response to an enable signal, and a test mode in which the latch is held open.

7. (original) A method as claimed in claim 6, further comprising the steps of:

inserting test data into the first combinational logic block when the electronic circuit is in the test mode; and

retrieving processed test data from the second combinational logic block;

wherein the test data is processed by the first and second combinational logic blocks as though they are a single combinational logic block.